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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,196	HOLSCHER ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the claims and remarks filed 12 January 2009. Claims 1-21 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-5, 7-12, 14, 16, 18 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Willke [US 6625696 B1] (hereinafter "Willke").

Per claim 1, Willke teaches a request tracking data prefetch apparatus for a computer system, comprising:

a prefetcher (see col. 2, lines 48-67, storage controller 110 which comprises control logic 112) coupled to a high latency memory for a processor of the computer system (see col. 2, lines 21-47, Storage Device 120 which can be DRAM or other types of high latency memory, requesting device 100 is a processor, see col. 1, lines 20-29 and Fig. 3);

a tracker within the prefetcher and configured to recognize accesses to a plurality of cache lines, wherein the accesses form a stream type sequential access pattern, and use a bit vector to predictively load a target cache line indicated by the stream-type sequential access pattern from the high latency memory into a low latency memory for the processor (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40, note that the buffer 114 contains a set of stored access patterns and prediction and accuracy values for each processor/requesting device, this set with the corresponding prefetching function in the storage controller 110 is construed to be a tracker; see col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines; see col. 3, lines 10-25, col. 7, lines 29-40 and col. 8, lines 30-35 for stream-type sequential access pattern; also see Fig. 5, items 510, 520, 540 and 560).

Per claim 9, Willke teaches a request tracking data prefetch apparatus for a computer system, comprising:

a processor (requesting device 100 is a processor, see col. 1, lines 20-29 and Fig. 3);

a system memory (see col. 2, lines 21-47, Storage Device 120 which can be DRAM or other types of high latency memory) coupled to the processor;

a prefetch unit (see col. 2, lines 48-67, storage controller 110 which comprises control logic 112) coupled to the system memory;

a plurality of trackers included in the prefetch unit, wherein the trackers are respectively configured to recognize accesses to pages of the system memory (note that Willke teaches DRAM, see col. 2, lines 29-45), and configured to recognize accesses to cache lines that form a stream type sequential access pattern; and

a cache memory coupled to the prefetch unit, wherein the prefetch unit uses a bit vector to predictively load target cache lines from the system memory into the cache memory to reduce an access latency of the processor, and wherein the target cache lines are indicated by the stream type sequential access pattern identified by the trackers (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40, note that the buffer 114 contains a set of stored access patterns and prediction and accuracy values for each processor/requesting device, this set with the corresponding prefetching function in the storage controller 110 is construed to be a tracker; see col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines; see col. 3, lines 10-25, col. 7, lines 29-40 and col. 8, lines 30-35 for stream-type sequential access pattern; also see Fig. 5, items 510, 520, 540 and 560).

Per claim 18, it should be clear that the instant claim is already substantially described by claims 1 and 9 as set forth above.

Per claims 2 and 10, Willke further teaches each of the trackers include a tag (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40; note that any configuration/setting data can be construed as a tag, and there are separate sets of prediction and accuracy values and stored access patterns for each processor) configured to recognize accesses to corresponding cache lines of the high latency memory by the processor (note that Willke teaches DRAM, see col. 2, lines 29-45, col. 6, line 52-67 and col. 7, lines 1-28).

Per claims 3 and 11, Willke further teaches a plurality of system memory accesses by the processor to the high latency memory as recognized by the tag are used by the trackers to determine the target cache line for a predictive load into the cache memory/low latency memory (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40 and the rejection of claims 1 and 9 set forth above; the stored access patterns are formed by multiple accesses by the corresponding processors).

Per claims 4 and 12, Willke further teaches accesses by the processor to adjacent cache lines of a page of the system memory are used to determined the target cache line of a stream type access pattern for a predictive load into the cache memory, wherein the adjacent cache lines have adjacent addresses, and wherein the target cache line is part of stream-type accesses that formed the stream-type access pattern (see col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines; see col. 3, lines 10-25, col. 7, lines 29-40 and col. 8, lines 30-35 for stream-type sequential access pattern and adjacent addresses).

Per claim 5, Willke further teaches the high latency memory comprises a memory block of a plurality of memory blocks of the computer system (see DRAM and disks, col. 2, lines 29-45, also see col. 6, line 52-67 and col. 7, lines 1-28; a memory block can be a cache line, a page, a byte, or any other unit of memory storage).

Per claims 7 and 14, Willke further teaches each of the plurality of trackers includes a tag configured to monitor a sub portion of the high latency memory block/page for accesses by the processor (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40; note that any configuration/setting data can be construed as a tag, and there are separate sets of prediction and accuracy values and stored access patterns for each processor; each of the stored access patterns only corresponds to a sub portion of the DRAM/the high latency memory).

Per claim 8, Willke further teaches the high latency memory is a system memory of the computer system (see DRAM, col. 2, lines 29-45).

Per claim 16, Willke further teaches that the cache memory is a prefetch cache memory within the prefetch unit (see Fig. 1, Buffer 114 is within Storage Controller 110).

Per claim 21, Willke further teaches said prefetch unit accesses to system memory are timed to utilize processor-to-system memory idle time (note that all memory accesses timed by a clock such as system clock in a digital computing system; also see col. 3, lines 10-25 and Fig.1 and 3, processor-to-system memory is idle during the time storage controller 110 accesses storage device 120 for prefetching and satisfying requesting device 100's requests, also storage controller 110 is only able to access

storage device 120 when the processor/requesting device 100 is not directly accessing the storage device 120.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willke.

Per claims 6 and 13, Willke does not specifically teach the system/high latency memory comprises a plurality of 4KB pages but teaches the high latency memory is a DRAM (see col. 2, lines 21-40). DRAM page sizes are determined by design choices and system specifications, and page sizes such as 4KB and 8KB are common in the art. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use 4KB as the page size in Willke's DRAM if dictated by design choice and system specification.

Per claim 15, Willke further teaches the cache line are 64 byte cache lines (see col. 7, lines 14-15) and a tag is used to monitor half of a page for accesses by the processor (here a page is broadly construed as an unit of storage that is twice the size of a cache line, also note that any configuration/setting data can be construed as a tag,

and there are separate sets of prediction and accuracy values and stored access patterns for each processor, see the rejection of claim 2 set forth above), but does not teach the cache lines are 128 bytes. However, it is clear that cache line sizes are design dependent and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make Willke's cache like size 128 bytes as a design choice.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Willke, further in view of Microsoft Computer Dictionary (hereinafter "Microsoft").

Per claim 17, Willke does not specifically disclose that the cache memory is an L2 cache memory, but teaches the higher latency is a DRAM as set forth above in the rejection of claim 1. However, Microsoft discloses that a L2 cache is faster than DRAM and Willke's cache memory is a lower latency memory as compared to the higher latency DRAM. Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make Willke's cache memory a L2 cache because it is faster than DRAM.

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willke, further in view of Brooks [6,081,868] (hereinafter "Brooks").

Per claim 19, Willke further teaches the computer system includes a plurality of processors (requesting devices 300 are processors, see col. 1, lines 20-29 and Fig. 3), but does not specifically disclose that each of the processors is coupled to a respective

high latency memory and a low latency memory. However, Brooks teaches a prefetch system wherein each of a plurality of processors is coupled to a respective high latency memory and a low latency memory (see Brooks: Fig 2, a CPU is coupled to a CPU private memory and a CPU cache in each CPU block; CPU Private Memory has higher latency than CPU Cache), in order to provide data storage exclusively for the associated CPU (Brooks: Col 5, Lines 25-30), higher performance and better fault tolerance. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to couple each of Willke's plurality of processors to a respective high latency memory and a low latency memory in order to provide data storage exclusively for the associated processor, increase performance and improve fault tolerance.

Per claim 20, the claim is already substantially disclosed by claims 4, 12 and 19 as set forth above.

Response to Arguments

8. Applicant's arguments with respect to claims 1-21 have been considered but are not persuasive. These arguments primarily focus on the limitation "use a bit vector to predictively load a target cache line" and the Applicant contends that Willke fails to teach this particular limitation. This Examiner respectfully disagrees.

Willke teaches predicting quantities of data and prefetching based on the prediction, wherein the quantities of data are measured in the number of cache lines (see Willke, col. 4, lines 59-67 and col. 5, Table 2). If the quantites of prefetched data can be at least a cache line in size, then clearly at least a cache line is the target of the

prefetch (hence "target cache line"). Furthermore, Willke specifically teaches that "the storage locations in cache memory 330 are commonly referred to as cache lines ... cache lines ... also store bits associating the address of the storage location within buffer 314 from which the prediction was retrieved and was used in reading the data from storage device 320 that filled each cache line ... association may be for individual cache lines, or may be for a plurality of cache lines associated as a set of c ache lines with the single prediction" (see Willke, col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines). Note that even though Willke may prefetch multiple cache lines as a result of a prediction, each individual cache line still needs to be addressed and read. A cache line that is addressed and read is a targeted cache line.

As for using a bit vector for prediction and prefetching, Willke teaches the buffer 114 contains a set of stored access patterns and prediction and accuracy values for each processor/requesting device (see Willke, col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40). Note that a bit vector here is reasonably interpreted as a collection of bits of variable size in absence of a more specific definition as provided by the Applicant's written description, and Willke's buffer 114 contains at least one bit vector that is either directly or indirectly used by the prediction and prefetching of target cache lines.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SHAWN X GU/

Shawn X Gu
Patent Examiner
Art Unit 2189

18 April 2009

/Matt Kim/

Supervisory Patent Examiner, Art Unit 2186